# Current Conveyors

## History, Theory, Applications and Implementation

Slides from:

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Prof Chris Toumazou

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  - Push pull topology
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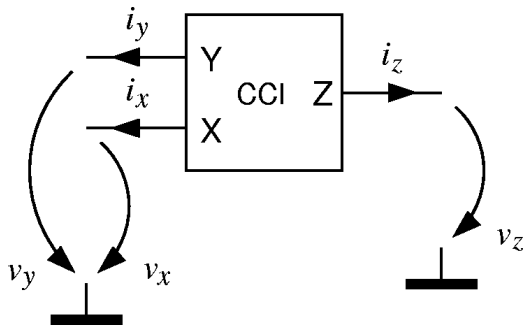
  - Instrumentation amplifier
- High-gain current conveyor CCII$\propto$
  - Example
- Third generation current conveyor CCIII
- References

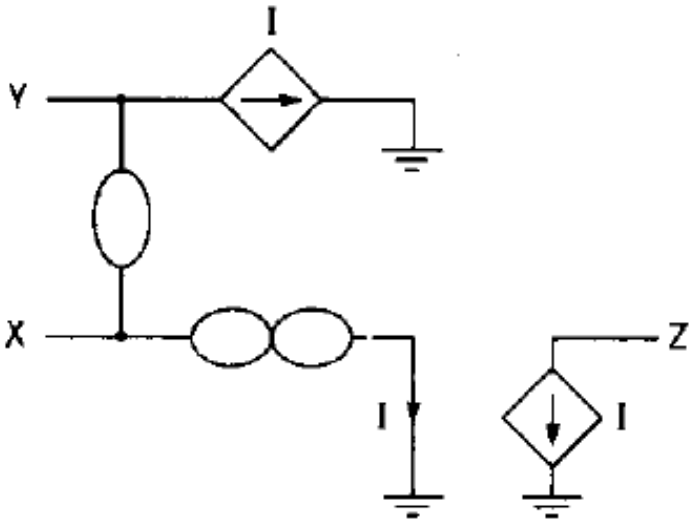
# Current conveyor




- Published by Sedra in 1968
- Four terminal device
- Open-loop current-mode amplifier with low and fixed current gain
  - The gain is set by transistor aspects or by controlling the impedance levels at the output or input
- Capable to convey current between two terminals (X and Z) with very different impedance levels
- Some advantages compared to op-amp
  - Can provide a higher voltage gain over a larger signal bandwidth than corresponding op-amp
  - Better CMRR in instrumentation amplifiers

# First generation current conveyor CCI

- If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X
- An input current I being forced into terminal X will result an equal amount of current flowing into terminal Y
- The current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance
- Potential of X being set by that of Y, is independent of the current being forced into port X
- Current through port Y being fixed by X is independent of the voltage applied to Y

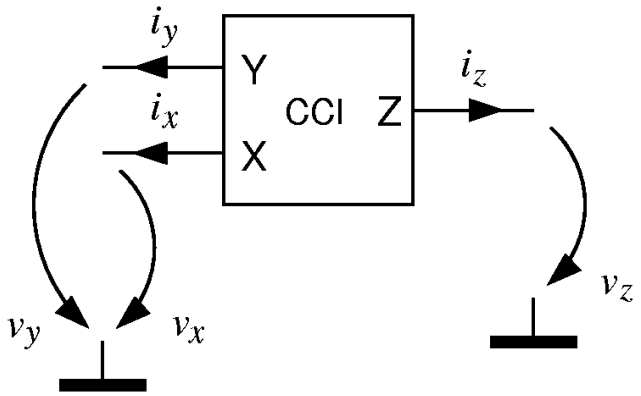


# First generation current conveyor CCI

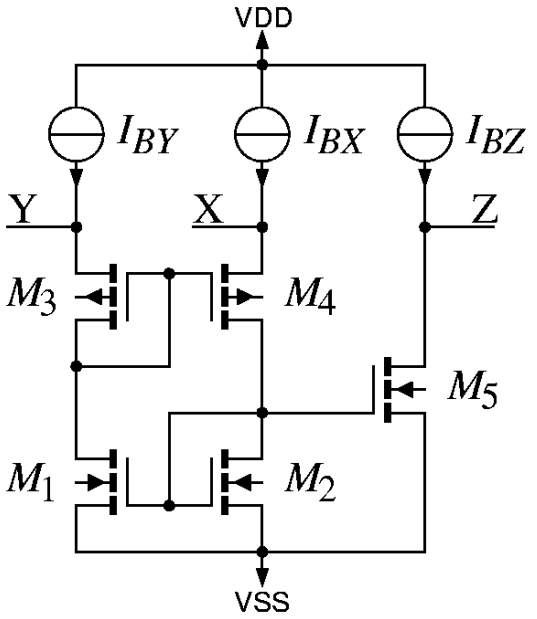
- Matrix representation

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

$$\Rightarrow \begin{cases} i_x = i_y = i_z \\ v_x = v_y \end{cases}$$

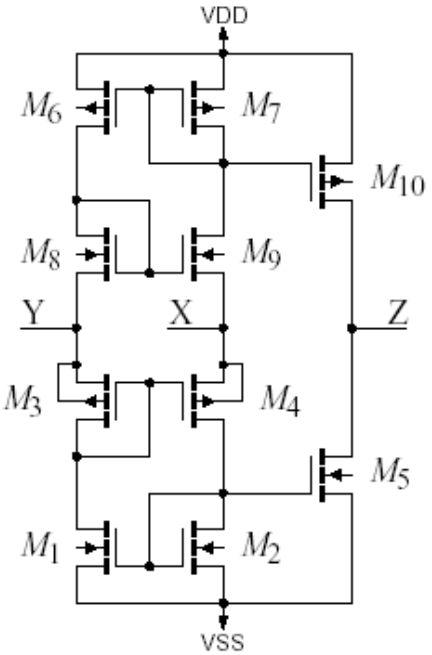


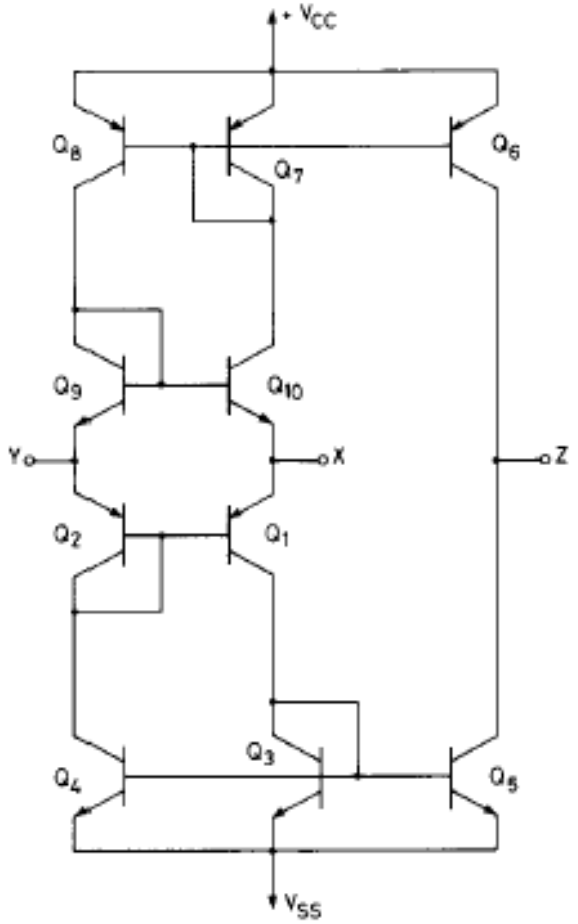

- MOS implementation
  - NMOS transistors $M_1$ and $M_2$ form a current mirror that forces the drain currents of the PMOS transistors $M_3$ and $M_4$ to be equal and hence the voltages at the terminals X and Y are forced to be equal



# Push-pull CCI topology

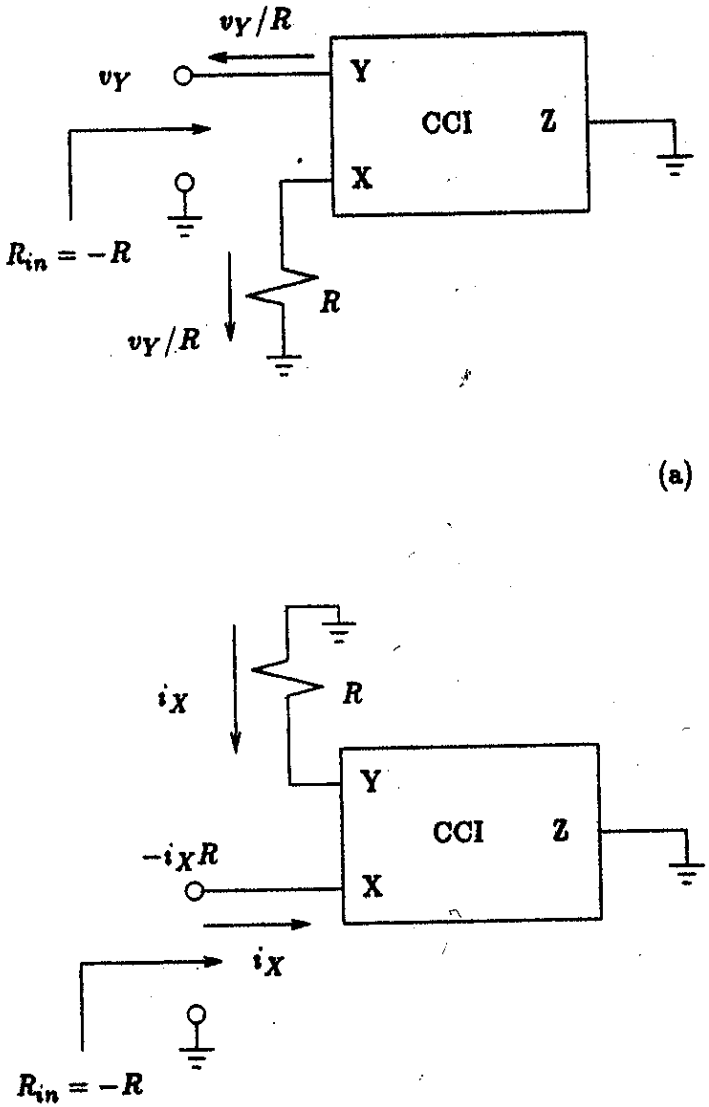
- Class AB circuit capable of bidirectional current operation
- Two complementary conveyors
- Bipolar implementation can be problematic due to the lack of high quality pnp devices



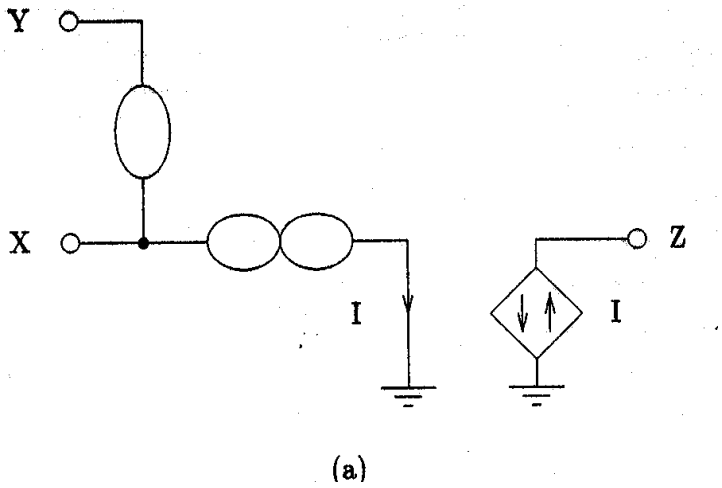
# Negative Impedance Converter

- Negative Impedance Converter (NIC)
  - If a resistor R is connected between X and ground the input impedance of the port Y is a voltage controlled negative resistance
  - If a resistor R is connected between Y and ground the input impedance of the port X is a current controlled negative resistance
- Can be useful in some applications like oscillators



# Second generation current conveyor CCII

- Published by Sedra in 1970
- If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X
- The current in node Y=0
- The current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I, with high output impedance
- Potential of X being set by that of Y, is independent of the current being forced into port X
- Terminal Y exhibits an infinite input impedance



(a)

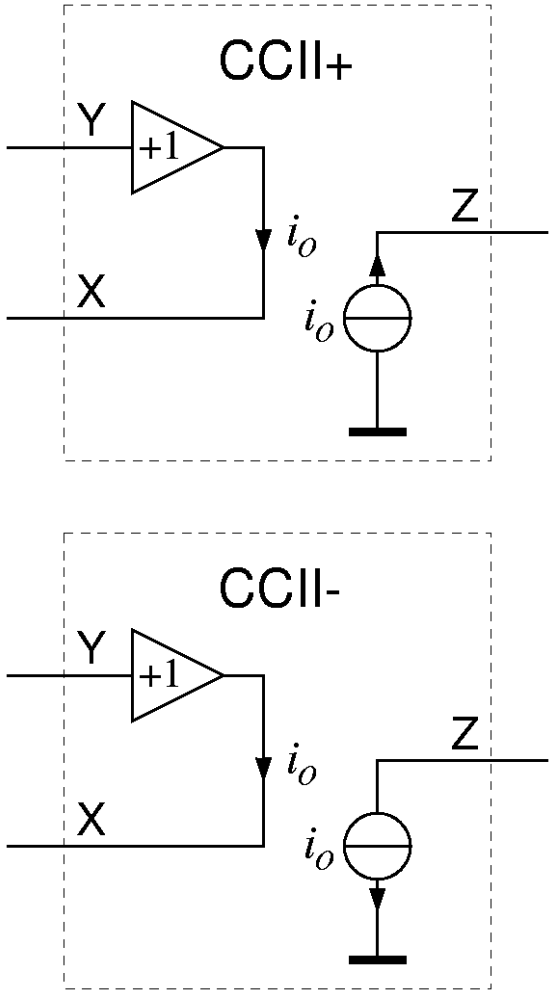
# Second generation current conveyor CCII

- Matrix representation

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$

$$\Rightarrow \begin{cases} i_y = 0 \\ v_x = v_y \\ i_z = \pm i_x \end{cases}$$

- CCII- may be viewed as an ideal MOS transistor
  - Y=gate, X=source, Z=drain



# AMPLIFIERS

## Current output stages.....

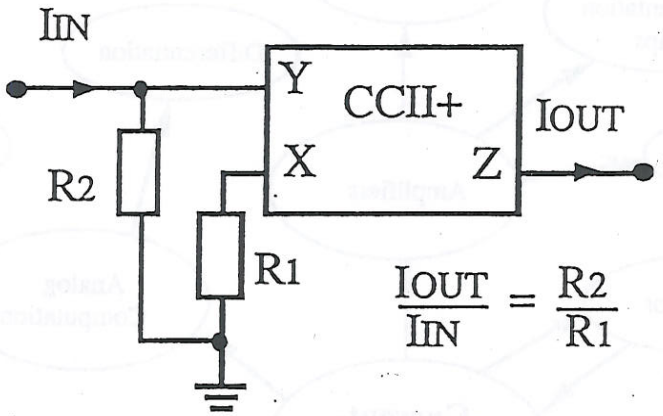



Figure 3a Current Amplifier (CCCS)

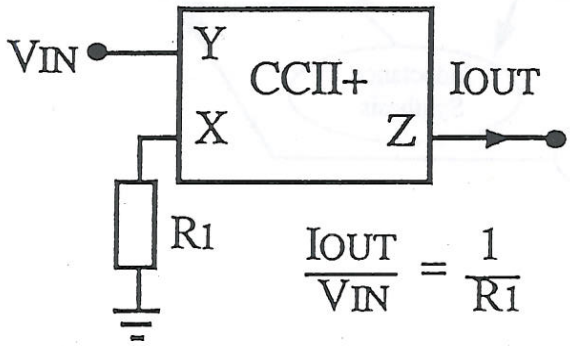



Figure 3b *V* to *I* Converter (VCCS)

AMPLIFIERS

current and voltage .....

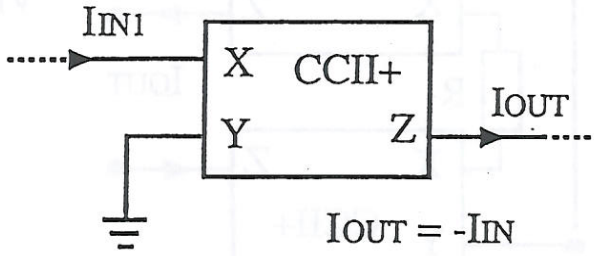



Figure 4 Current-Buffer or Current-Follower

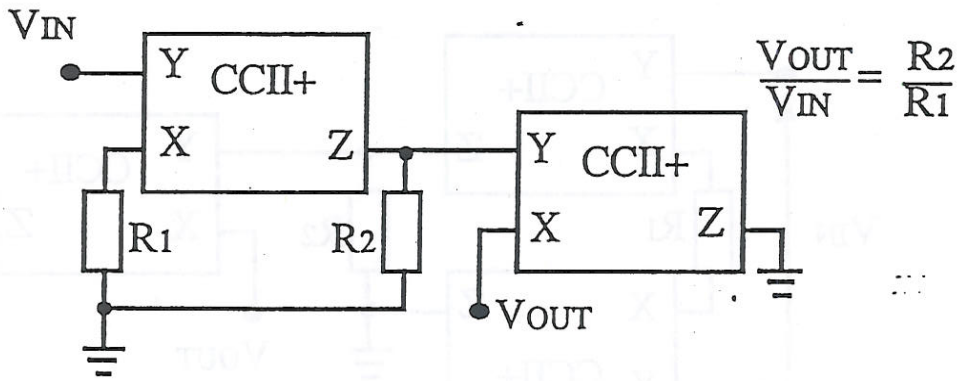



Figure 5 Voltage Amplifier

# AMPLIFIERS

## differential input/output stages.....

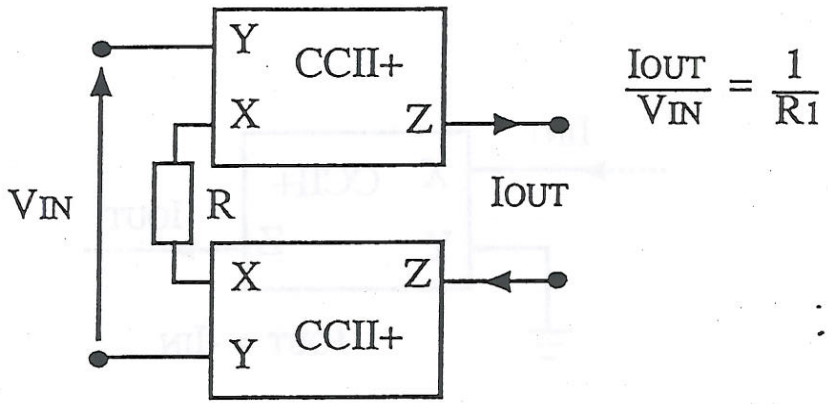



Figure 6 Differential *V* to *I* Converter

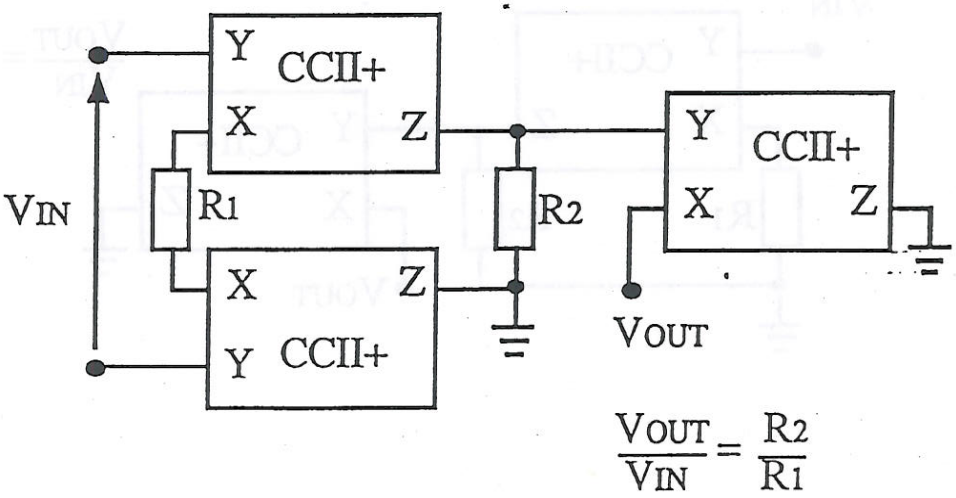



Figure 7 Instrumentation Amplifier

# ANALOG COMPUTATION

## current summing.....

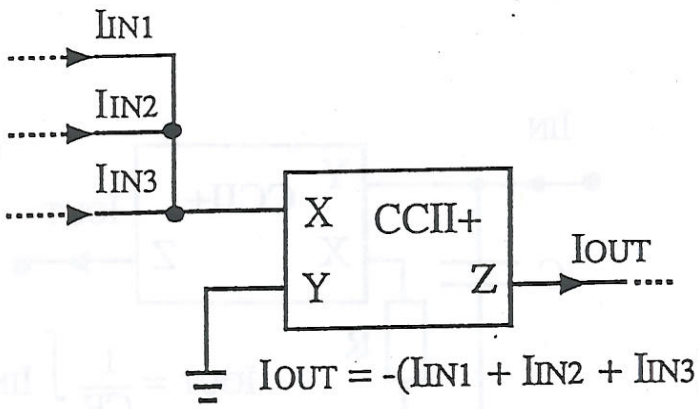



Figure 8a

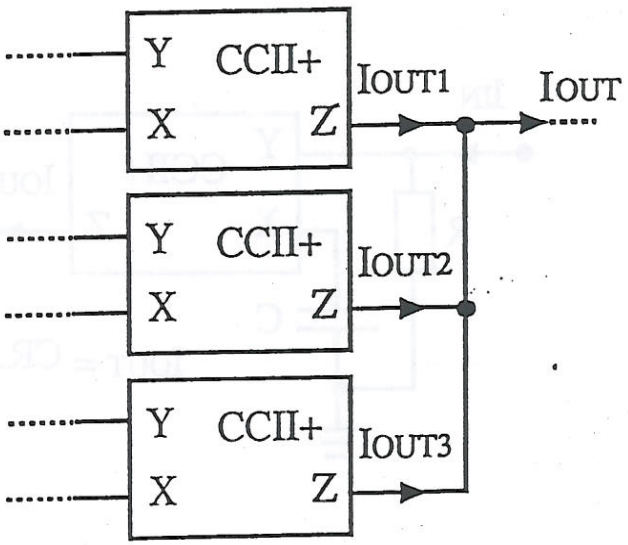



Figure 8b

# ANALOG COMPUTATION

## current integration and differentiation.....

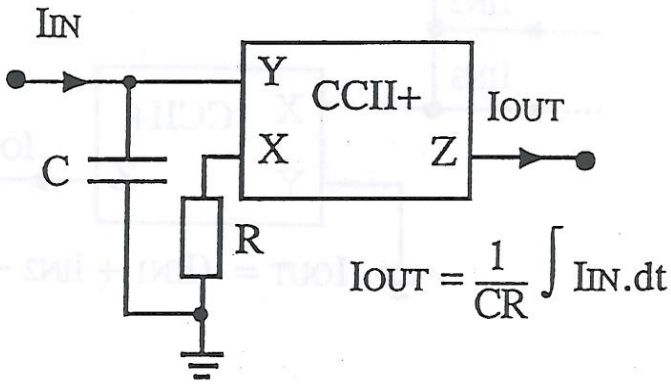



Figure 9a Current Integrator

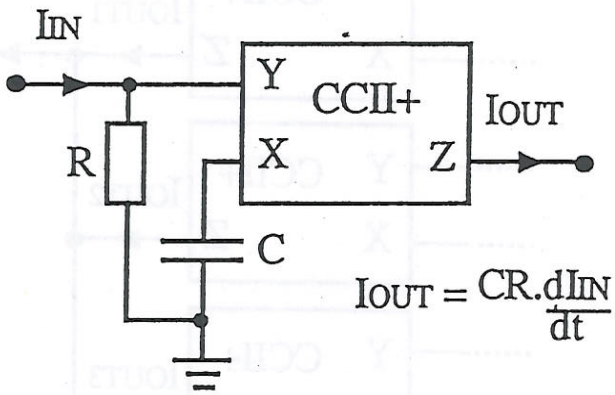



Figure 9b Current Differentiator

# ANALOG COMPUTATION

## voltage integration and differentiation.....

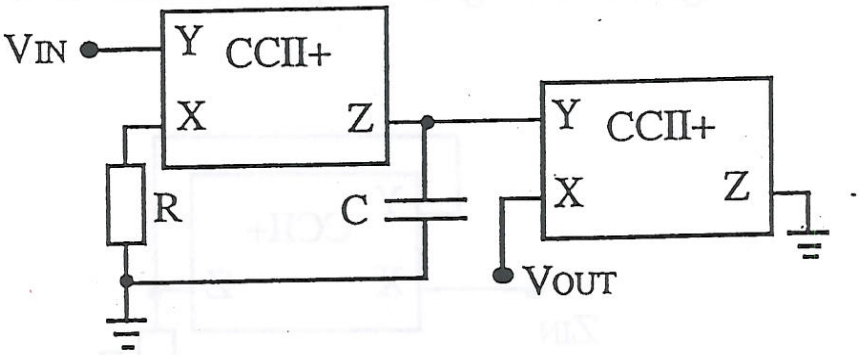



Figure 10a Voltage Integrator

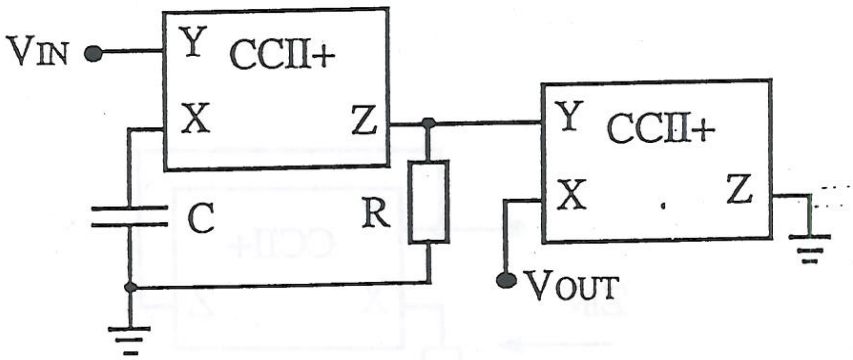



Figure 10b Voltage Differentiator

# NEGATIVE IMPEDANCE CONVERTERS

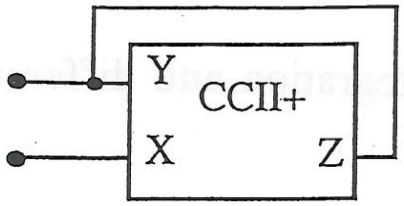



Figure 11a Negative Impedance Converter (NIC)

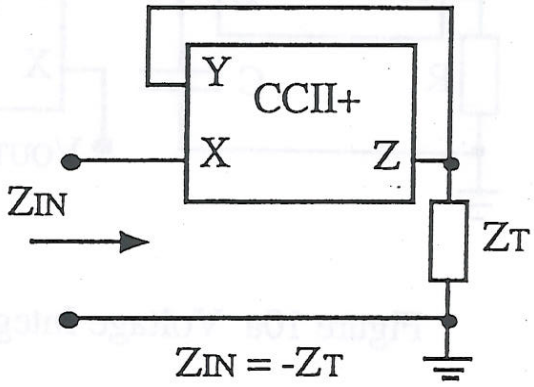



Figure 11b Current-Controlled NIC

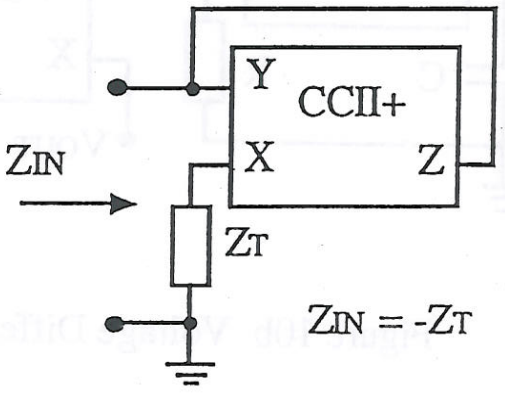



Figure 11c Voltage-Controlled NIC

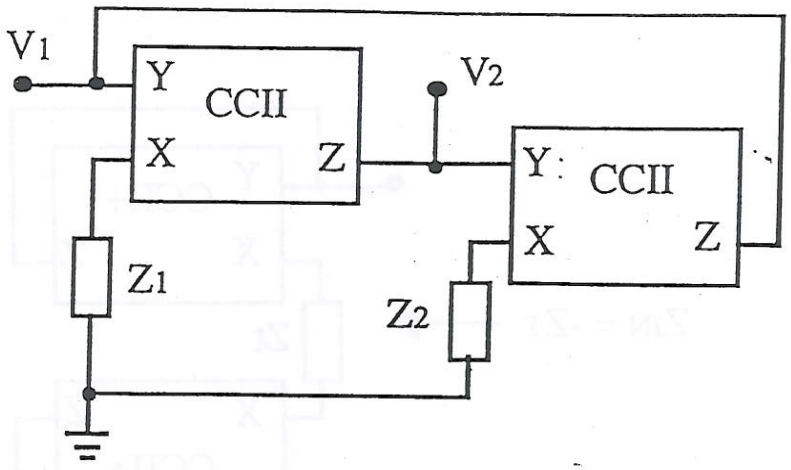



Figure 12 Generalised Impedance Converter (GIC)

Both CCs same type then..... $Z_{IN} = Z_1.Z_2/Z_3$

or

If CCs opposite type then..... $Z_{IN} = -Z_1.Z_2/Z_3$

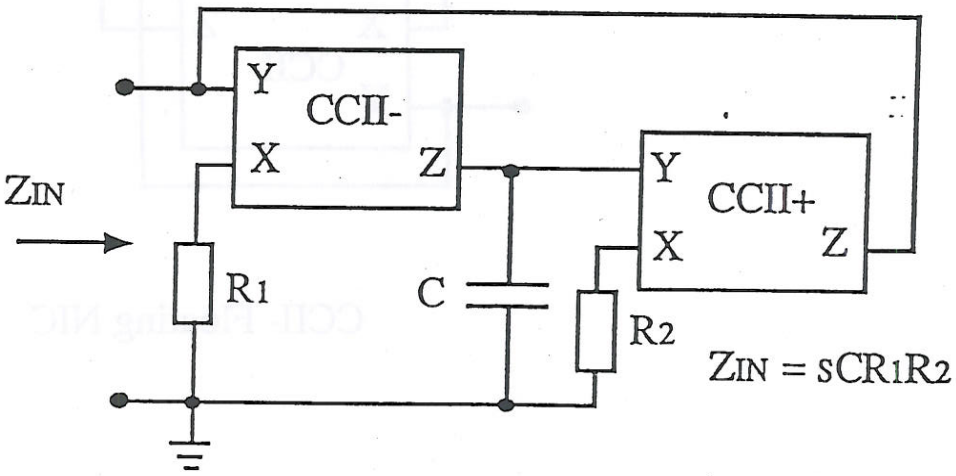
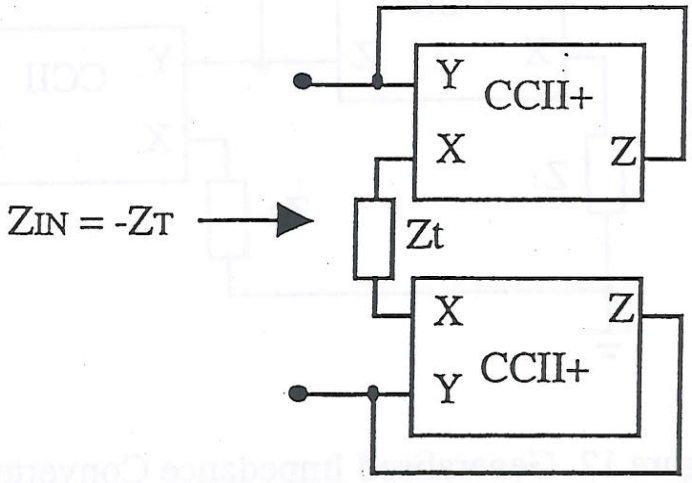
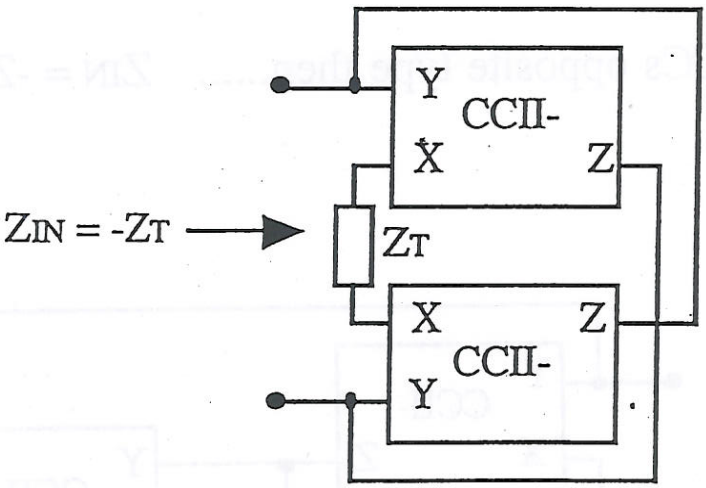



Figure 13 Simulated Grounded Inductance

# FLOATING NEGATIVE IMPEDANCE CONVERTERS



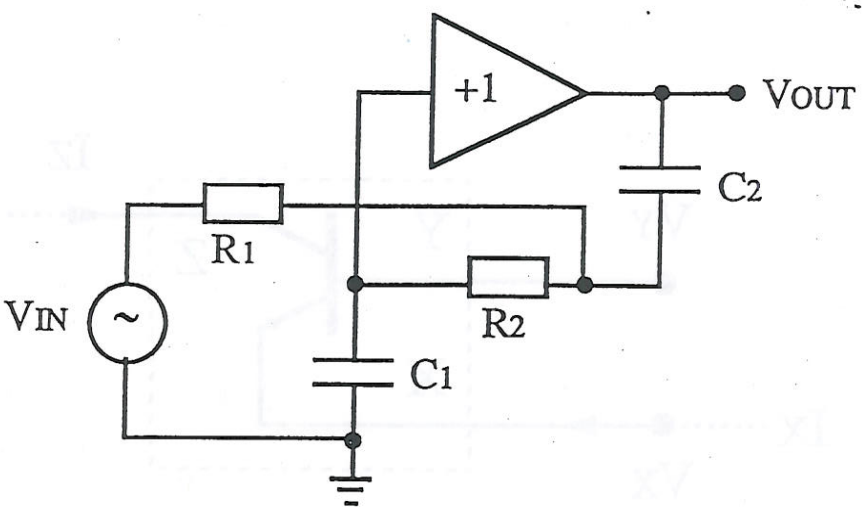

CCII+ Floating NIC



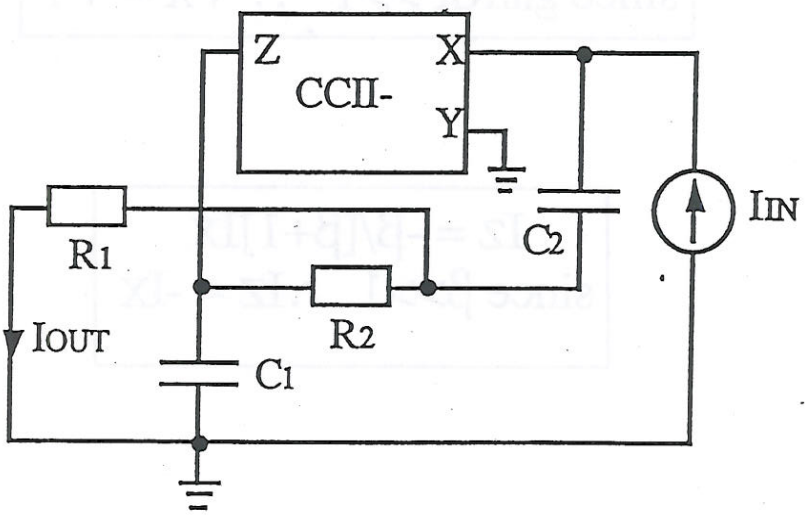

CCII- Floating NIC

# FILTERS

## Sallen-Key active biquad .....

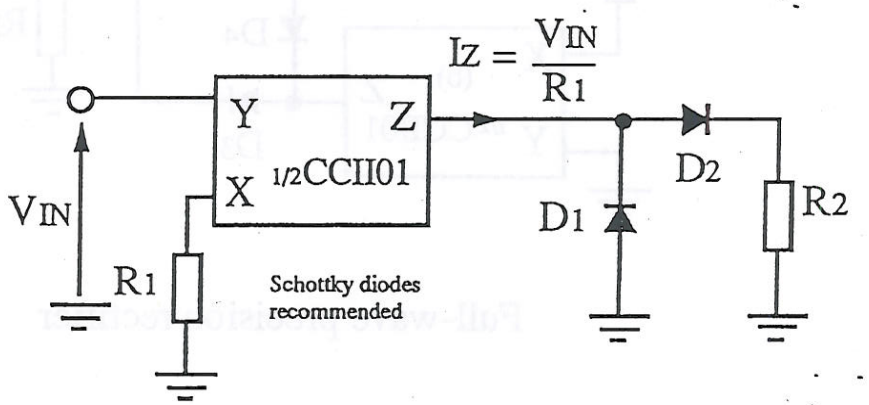



Voltage-Follower Sallen-Key Active Biquad

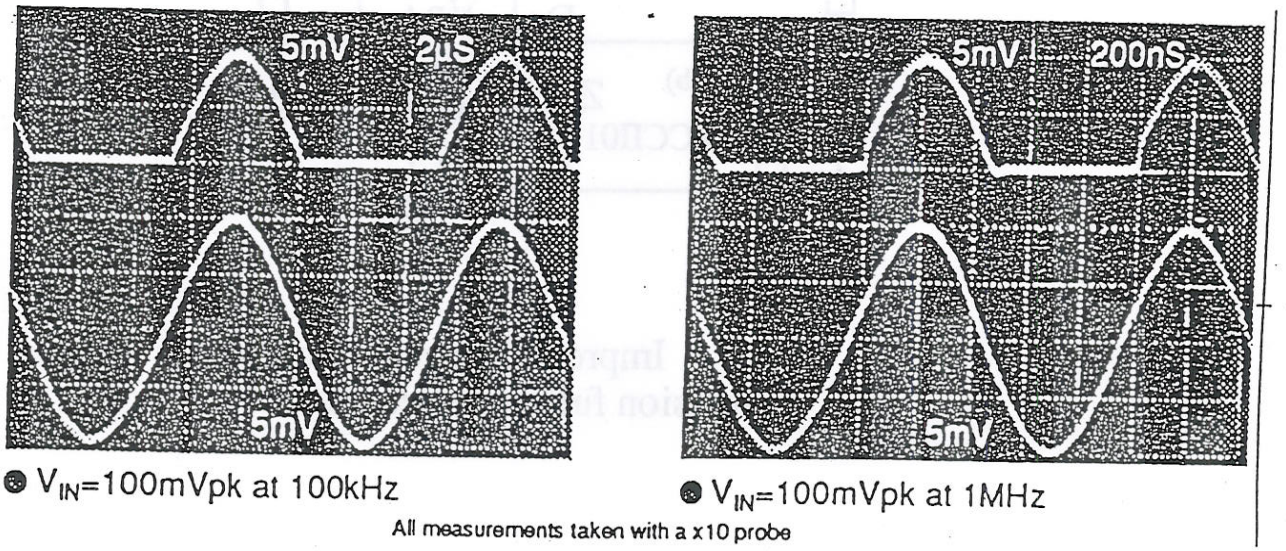



Current-Follower Sallen-Key Active Biquad

# PRECISION HALF-WAVE RECTIFIER



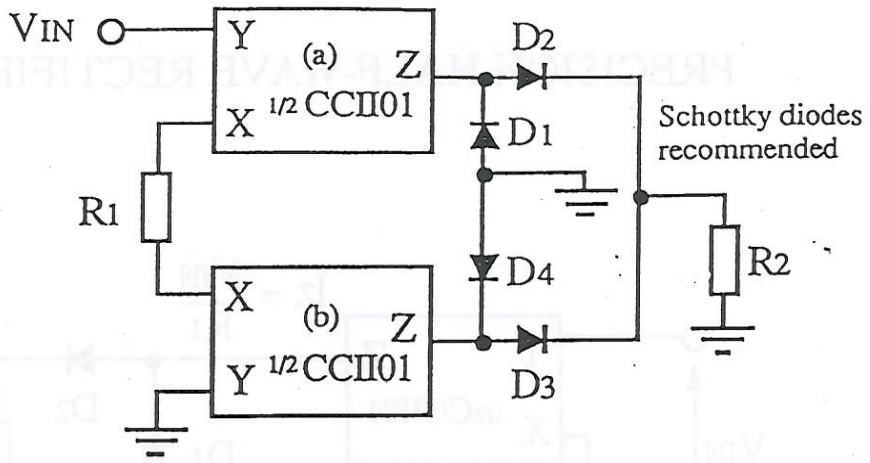

(a) Half-wave precision rectifier



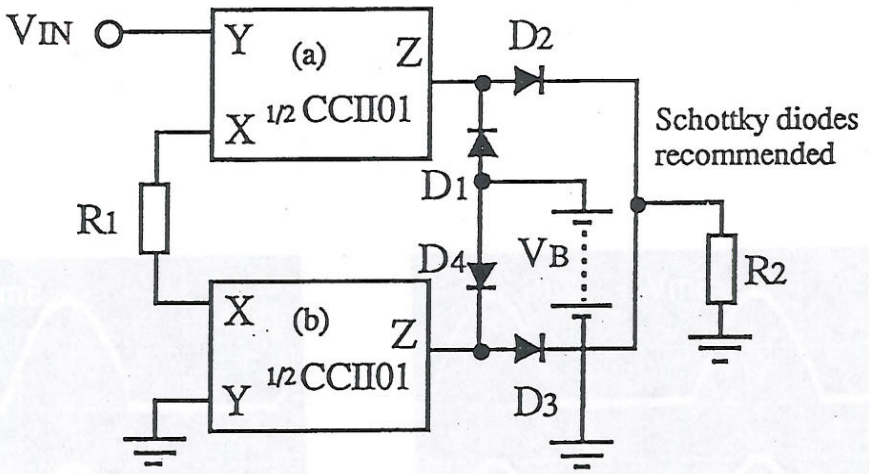

● $V_{IN}$=100mVpk at 100kHz ● $V_{IN}$=100mVpk at 1MHz

All measurements taken with a x10 probe

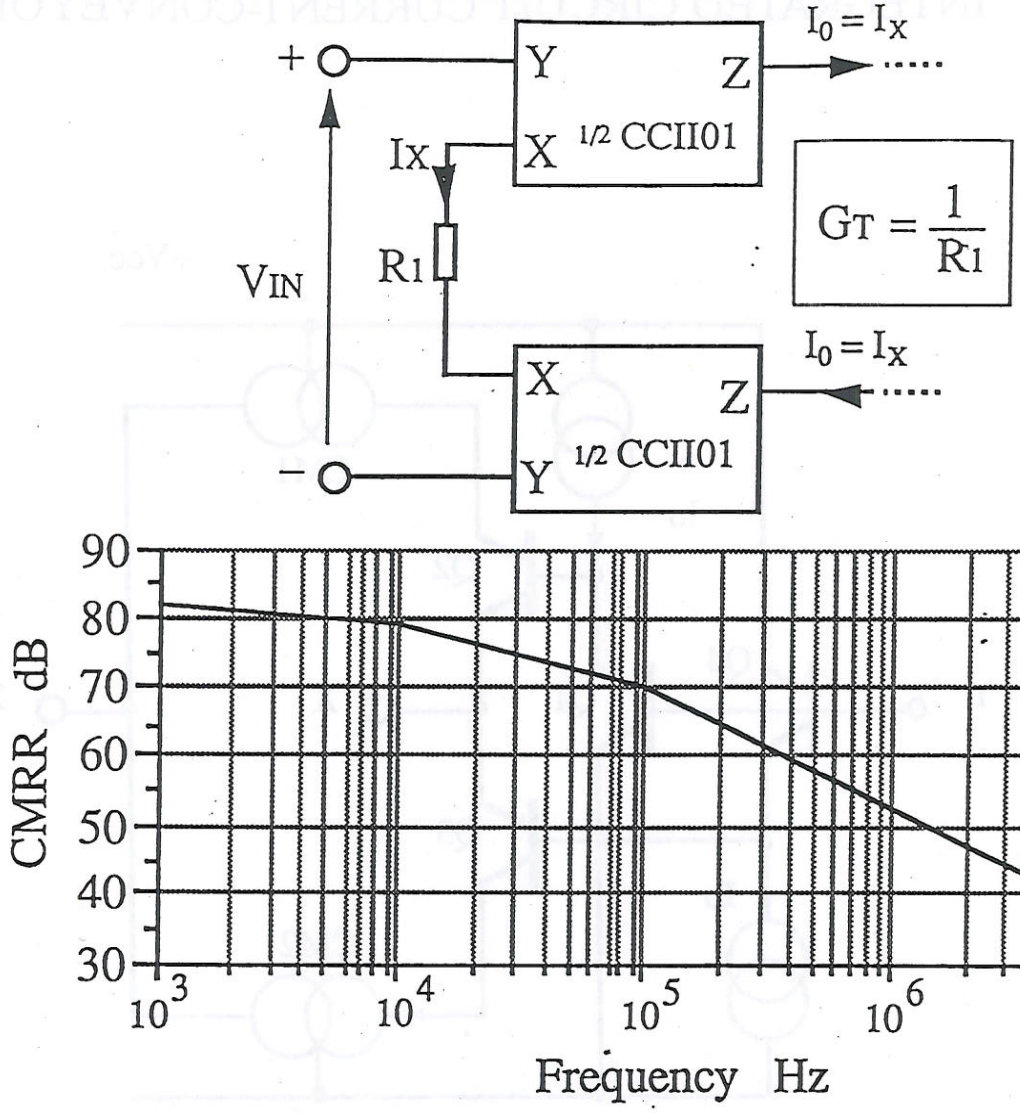
CCII01 Precision half-wave rectifier waveforms



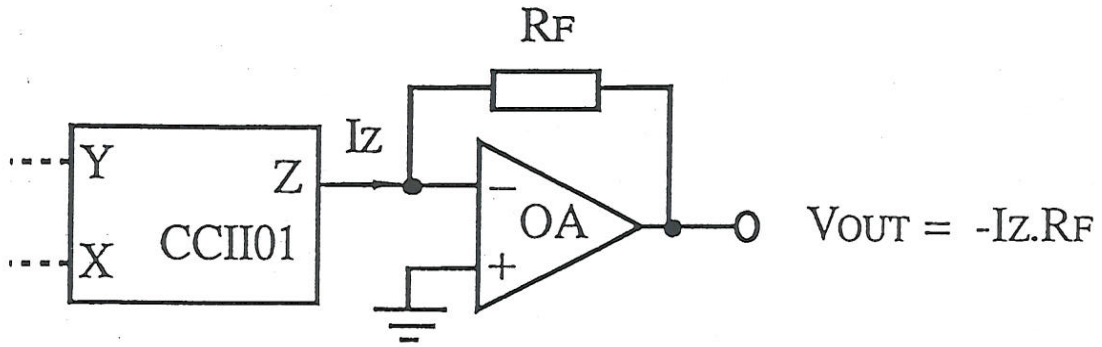

Full-wave precision rectifier




Improved current-conveyor
precision full-wave rectifier




CCII01 Instrumentation Amplifier



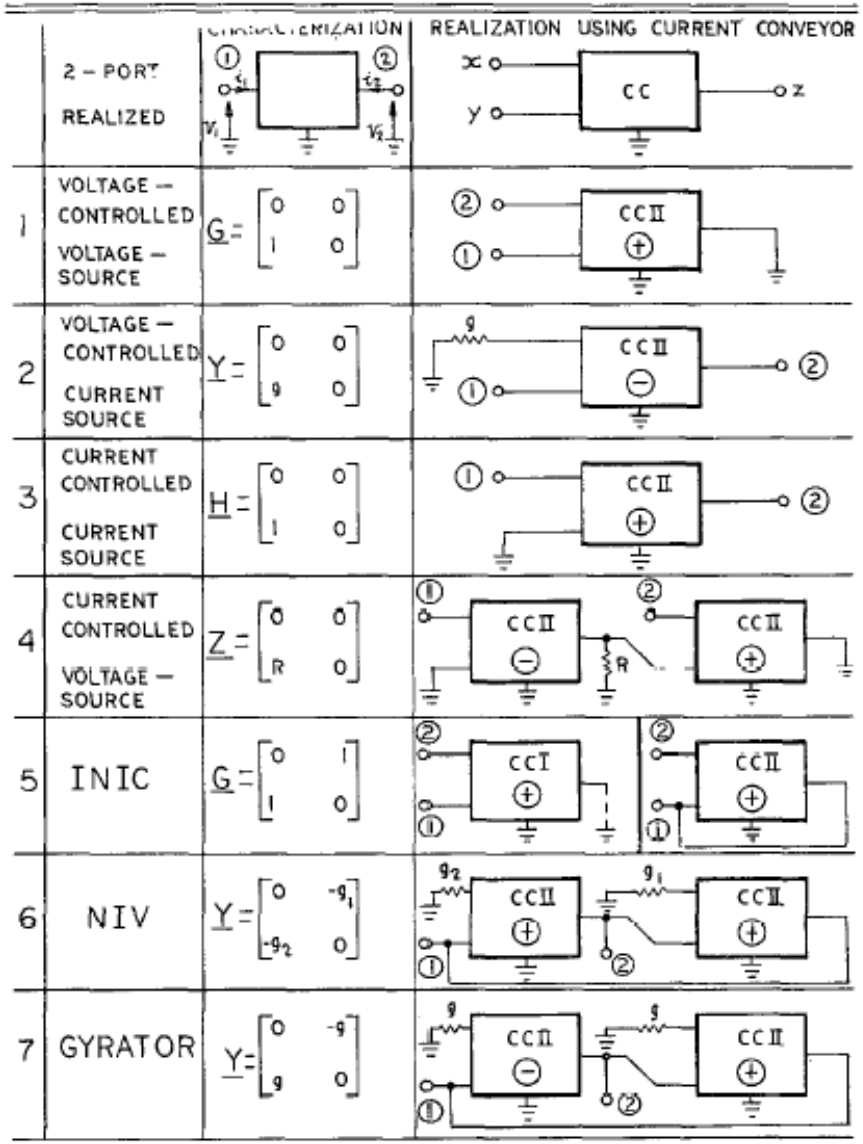

Transresistance Conversion of *Iz*

# Applications

- Applications for network synthesis
  - Controlled sources
  - Impedance converter
  - Impedance inverter
  - Gyrator

TABLE I

APPLICATION OF CURRENT CONVEYORS TO ACTIVE NETWORK SYNTHESIS

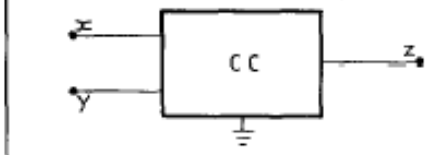
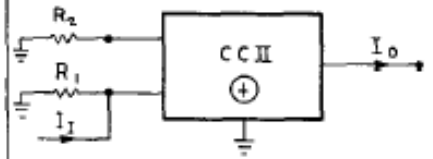
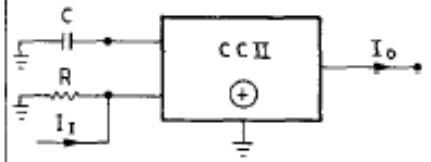
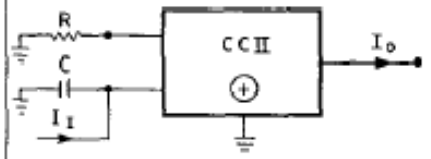
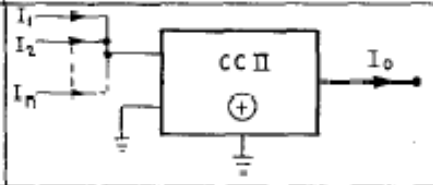
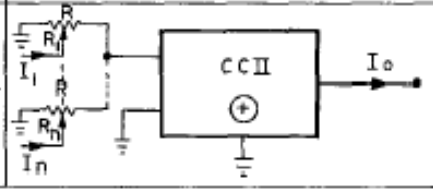


# Applications

- Applications to analog computation
  - Amplifier
  - Differentiator
  - Integrator
  - Summer
  - Weighted summer

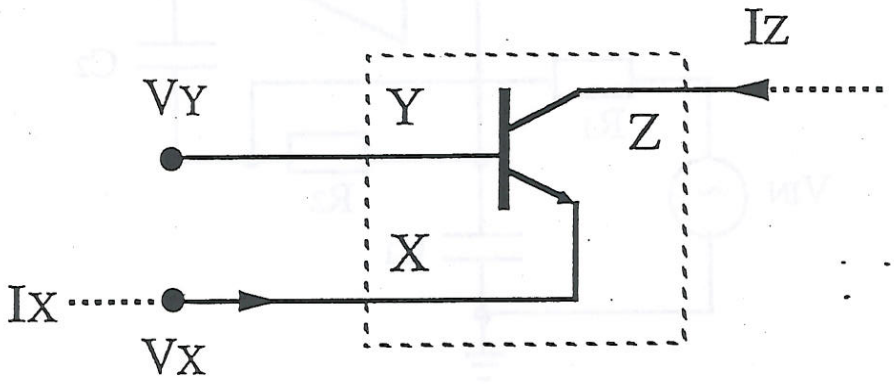
TABLE II

APPLICATION OF CURRENT CONVEYORS TO ANALOG COMPUTATION

| | FUNCTIONAL ELEMENT | FUNCTION | REALIZATION USING CURRENT CONVEYOR |
|---|---|---|---|
| | | |   |
| 1 | CURRENT — AMPLIFIER | $I_o=(R_1/R_2)I_1$ |   |
| 2 | CURRENT — DIFFERENTIATOR | $I_o=CR\frac{dI_1}{dt}$ |   |
| 3 | CURRENT — INTEGRATOR | $I_o=\frac{1}{CR}\int I_1 dt$ |   |
| 4 | CURRENT — SUMMER | $I_o=-\sum_1^n I_j$ |   |
| 5 | WEIGHTED CURRENT SUMMER | $I_o=-\sum_1^n I_j\frac{R_j}{R}$ |   |

# HOW DO WE CREATE A CURRENT-CONVEYOR?

Consider an ideal BJT .....




$$V_X \approx \frac{V_Y}{[1 + (1/g_m R_X)]}$$

since $g_m R_X >> 1 \quad \therefore V_X \approx V_Y$

$$I_Z = -\beta/[\beta+1] I_X$$

since $\beta >> 1 \quad \therefore I_Z \approx -I_X$

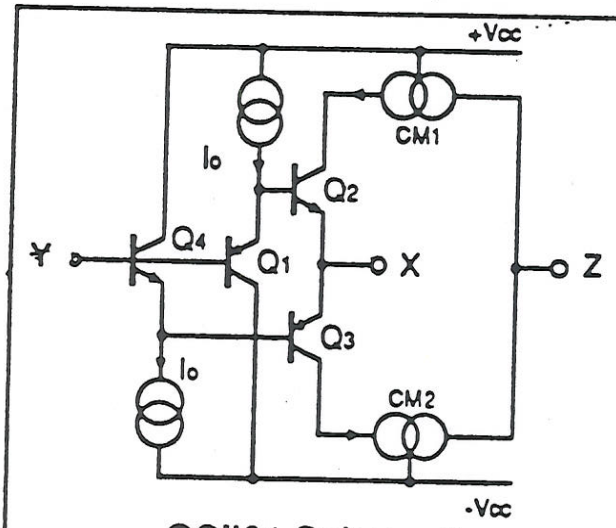
Single BJT CCII-

# CCII01

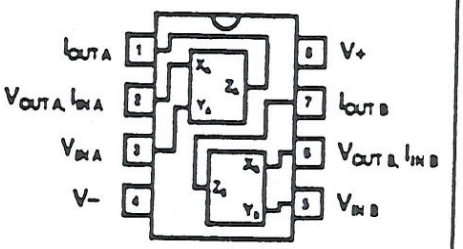
## Current Conveyor Amplifier

### The device

- Built with state-of-art complementary bipolar process
- Open-loop operation
- High speed performance guaranteed




CCII01 Schematic

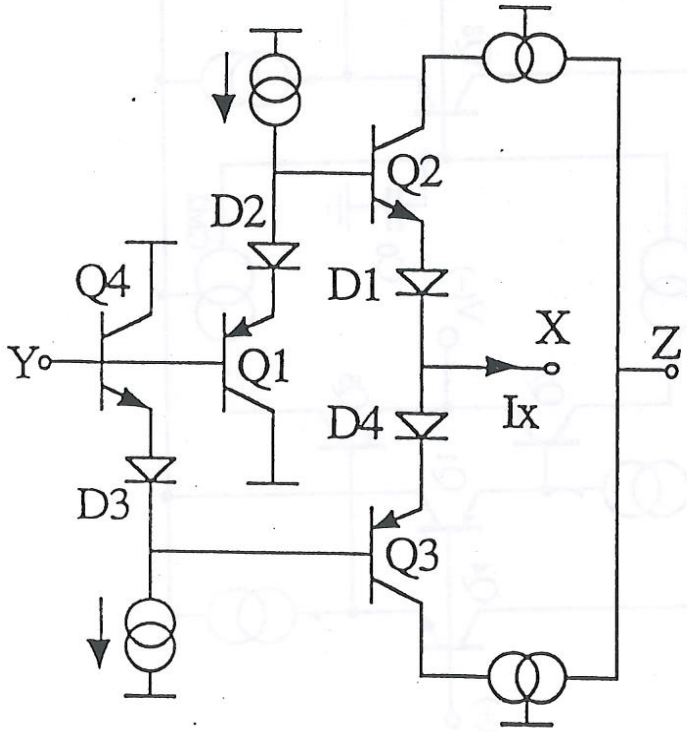



CCII01
Dual chip

### Key parameters

- 2000V/µs slew-rate
- 700 MHz equivalent gain-bandwidth product
- CMRR performance better than 53dBs at 1MHz
- Virtual ground impedance less than 50mΩ at 1kHz
- ±10mA max output current
- 80dBs equivalent open-loop gain
- Operation down to ± 5v supply

# Improved DC Input Matching Using Diodes

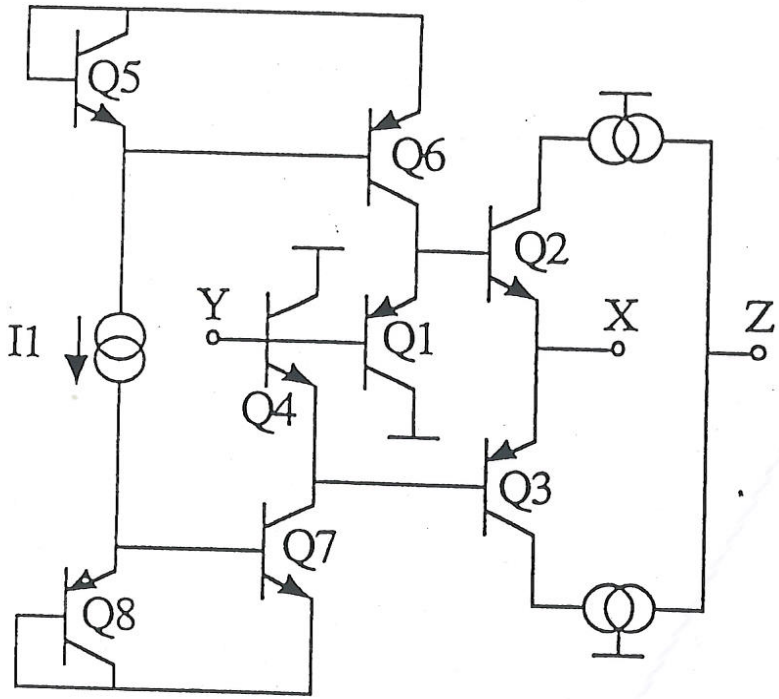



- $V_X - V_Y = (V_{BE1} - V_{D1}) - (V_{BE2} - V_{D2})$
- Quiescent offset $\Delta V \approx 0$
- Small-signal offset $\partial V = I_X R_X$

  $R_X = (re2+rd1) \parallel (re3+rd4)$

- Quiescent offset is reduced, but $R_X$ is increased

# Input Bias Current Scaling




- $V_X - V_Y = V_{BE1} - V_{BE2}$

$V_{BE6} = V_{BE5} = V_T \ln(I_1/I_{Sn})$

$I_{C1} \approx I_{C6} = I_{sp} \exp(V_{BE6}/V_T)$

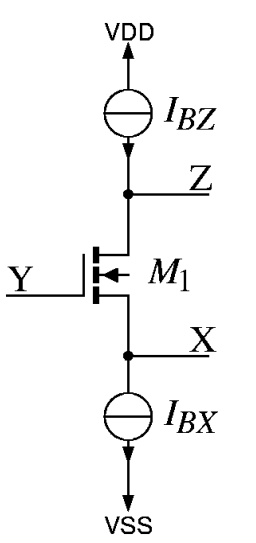
- $V_{BE1} = V_T \ln(I_{C1}/I_{sp})$
  $= V_T \ln(I_1/I_{sn})$

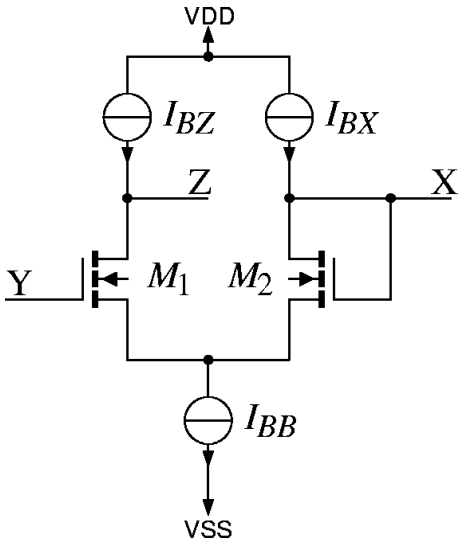
- $V_{BE4} = V_T \ln (I_1/I_{sp})$

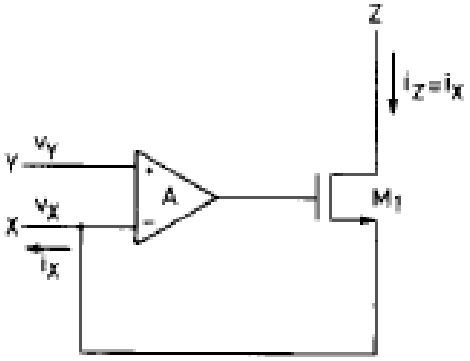
- Quiescent offset $\Delta V \approx 0$
- Small-signal $\partial V = I_x R_x$, $R_x = (re2 \parallel re3)$

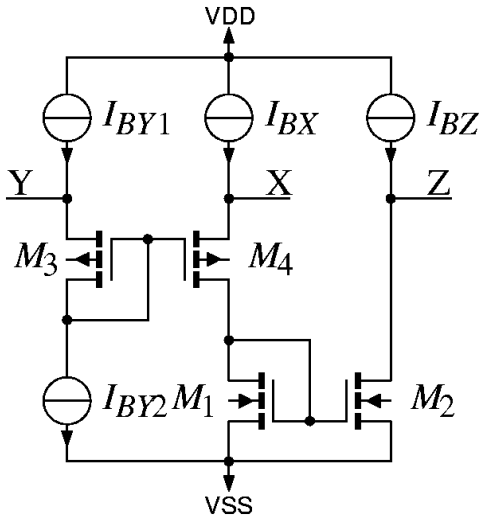
# MOS CCII realisations

- Negative current conveyor CCII-
  - Simplest realisation one NMOS-transistor with a current bias
    - $V_{gs1}$ shift between X and Y
  - Can be avoided by an additional level shifting transistor
  - NMOS in negative feedback loop of an op-amp
- Positive current conveyor CCII+
  - Similar to CCI with higher input impedance



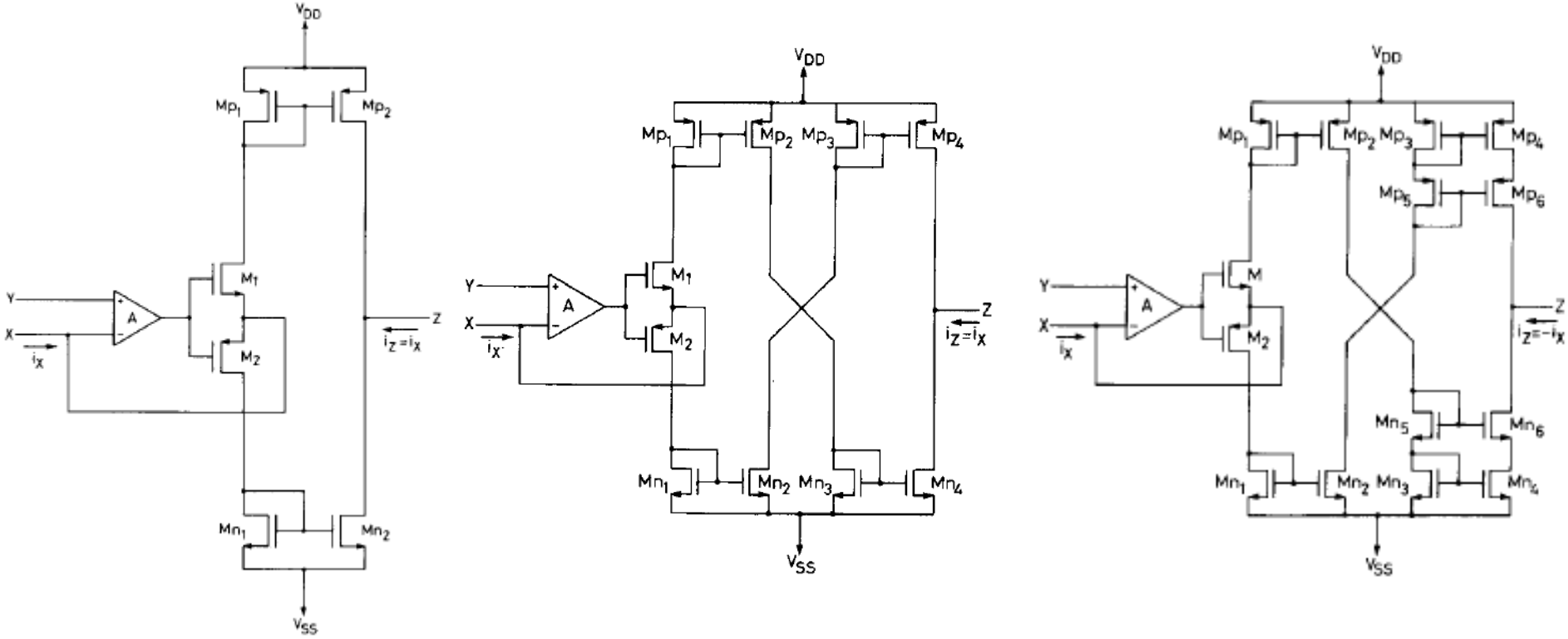



# 5μm CMOS CCII implementation (1/3)

- Three different CCII implemented
  - CII+, CII- with simple mirrors and CII- with cascode mirrors
    - Output swing ⇔ output impedance and accuracy trade off
    - In CII- structures the input voltage of the additional mirrors are not restricted to low voltages
  - Birectional current flow



# 5μm CMOS CCII implementation (2/3)

- Two stage operational amplifier with an additional output impedance stage
  - The output transistors $M_{10}$ and $M_{11}$ are the $M_1$ and $M_2$ in the CCII schematics

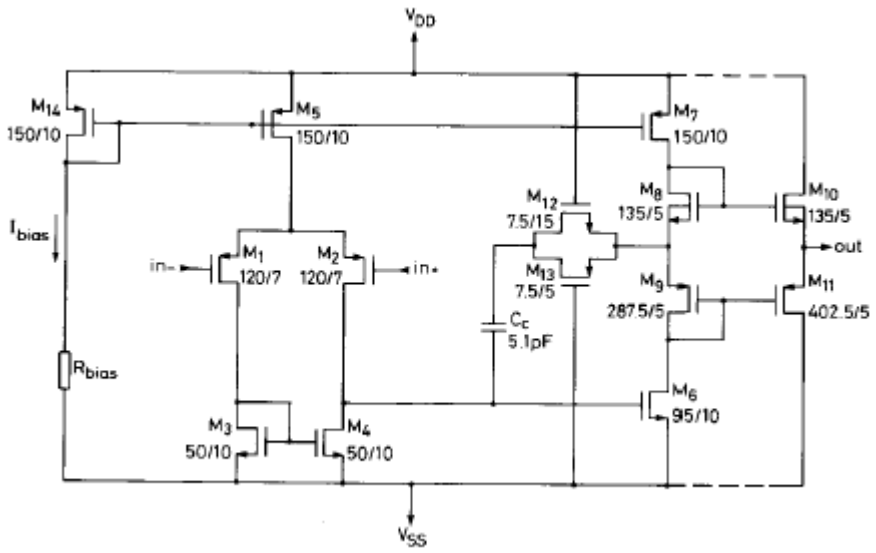



**Table 1: Measured CMOS op amp parameters**

| Parameters | Experimental results ($I_s$ = 25 μA) | Units |
|---|---|---|
| Open loop gain (50 Hz) | 72.7 | dB |
| Output resistance | 1051 | Ω |
| 3 dB frequency | 400 | Hz |
| Unity gain frequency | 2.2 | MHz |
| Slew rate (pos) | +2.26 | V per μsec |
| Slew rate (neg) | −6.87 | V per μsec |
| Power dissipation | 1.21 | mW |
| Input offset voltage | 17.4 | mV |
| PSRR | | |
| 100 Hz | 68.3 | dB |
| 10 KHz | 47.8 | dB |
| 500 KHz | 13.1 | dB |

# 5μm CMOS CCII implementation (3/3)

- Measurement results
  - The maximum voltage difference between Y and X below 8mV over the linear operation range
  - The Effective unity-gain-bandwidth product of the conveyor circuits is larger than the gain-bandwidth product of the op-amp

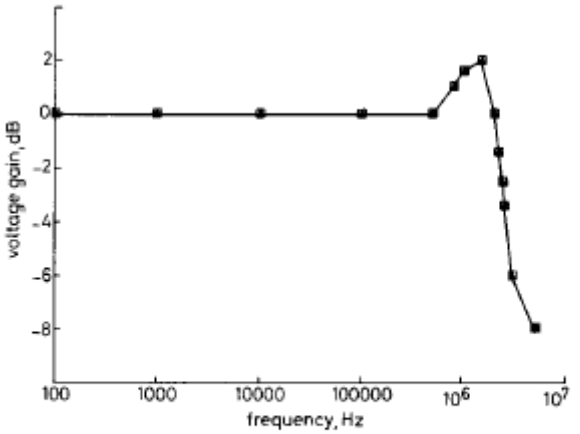



**Fig. 14** *Measured small-signal magnitude response of the voltage gain between terminals X and Y*

● = CCII +
△ = CCII – (simple mirrors)
□ = CCII – (stocked mirrors)

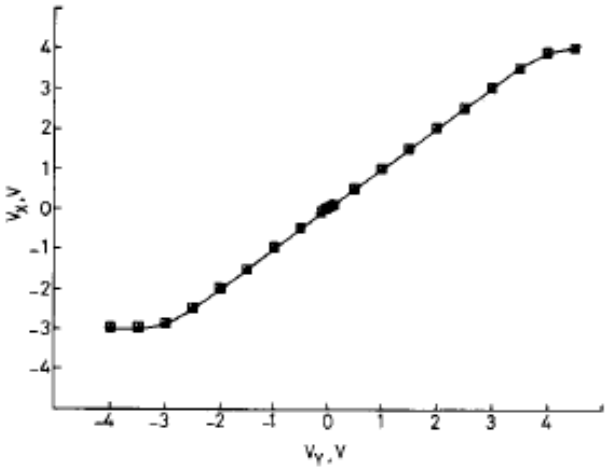



**Fig. 13** *Measured large signal voltage characteristics between terminals Y and X for the positive and negative current conveyors*

● = CCII +
△ = CCII – (simple mirrors)
□ = CCII – (stocked mirrors)

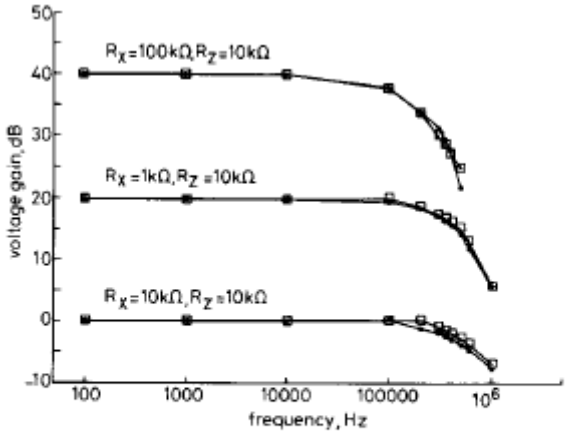
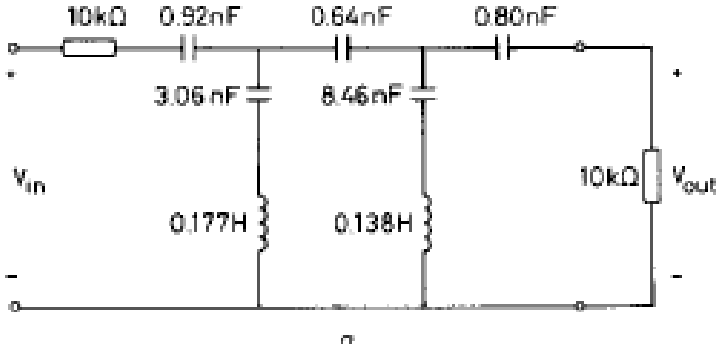



**Fig. 16** *Measured small-signal magnitude response of the voltage gain between terminals X and Z of an inverting amplifier with gain defined by $R_Z/R_X$*

● = CCII +
□ = CCII – (stacked mirrors)

# Grounded gyrator

- 5th-order High-pass elliptic LC-ladder filter using gyrator
  - Inductances of the filter are replaced with current conveyor gyrators
- The measured $L_{eq}=0.85C_2R_{12}R_{21}$



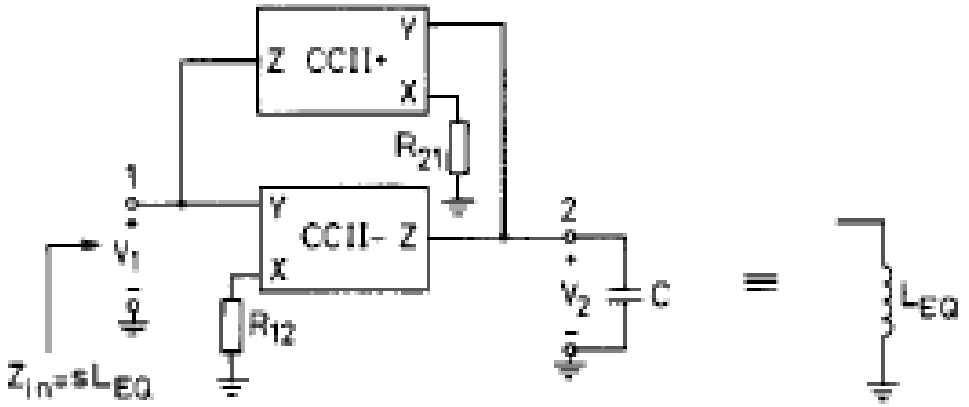
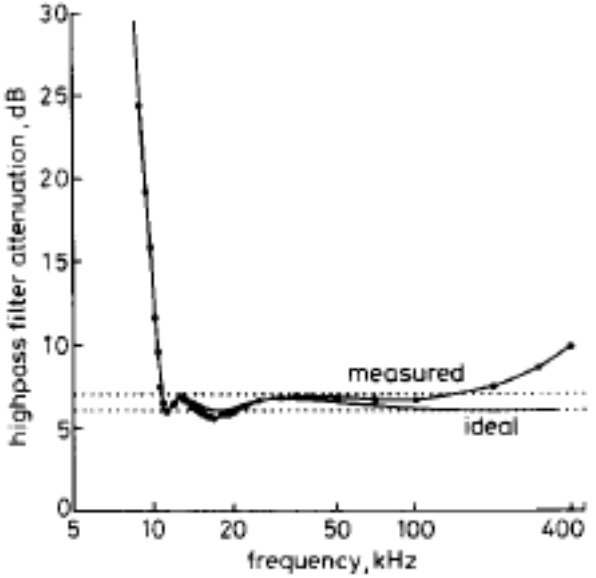




**Fig. 17** *Grounded gyrator realisation using current conveyors*



# Adjoint networks

- N and its adjoint network Na are Interreciprocal if $V_{out}/V_{in}=I_{out}/I_{in}$
  - N and Na are not necessarily the same circuit
- Provides a connection between well-known active-RC circuits and current conveyor based circuits
- Voltage amplifier with infinite input impedance and zero output impedance transforms into a current amplifier with zero input impedance and infinite output impedance

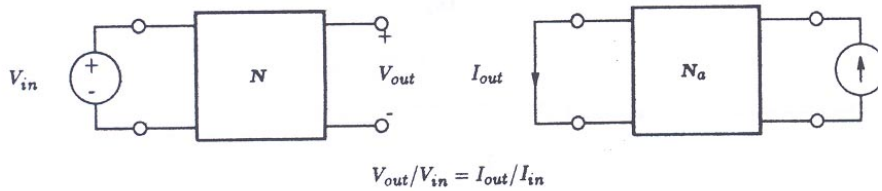
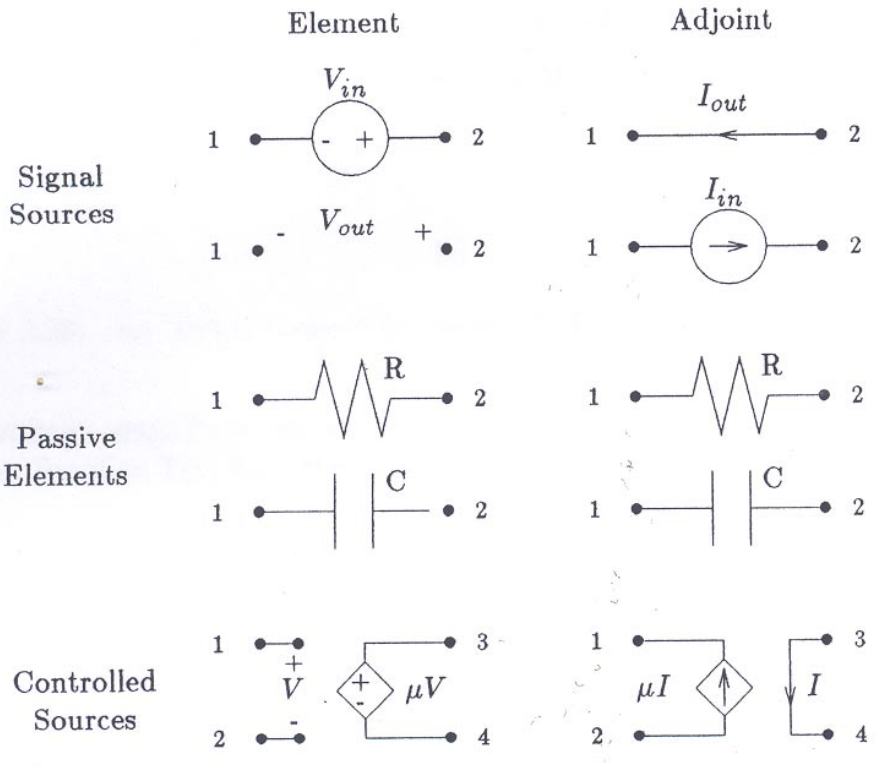



**Figure 3.23: Networks N and $N_a$ are interreciprocal to one another. and $N_a$ are not necessarily the same network.**



# Example, Sallen key

- Using the adjoint principle the low-pass Sallen-Key circuit can be replaced with a current conveyor based circuit
  - The transfer function is the same for both of the circuits

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} = \frac{4kQ^2 / R^2C^2}{s^2 + 2/RC\left[2Q(1-K)+1\right]s + 4Q^2 / R^2C^2}$$

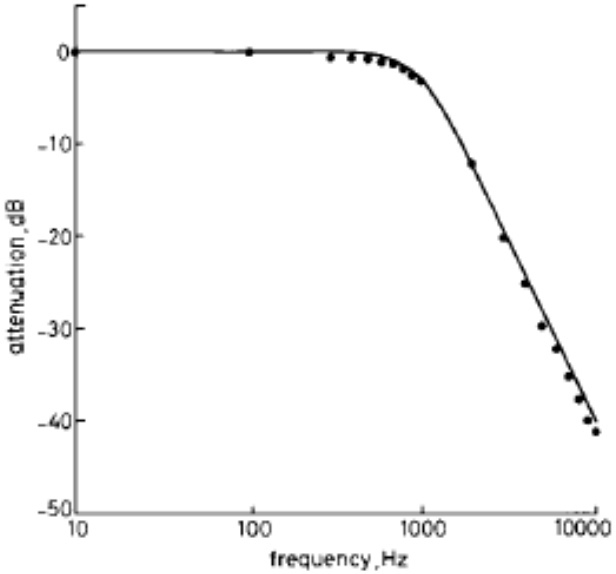
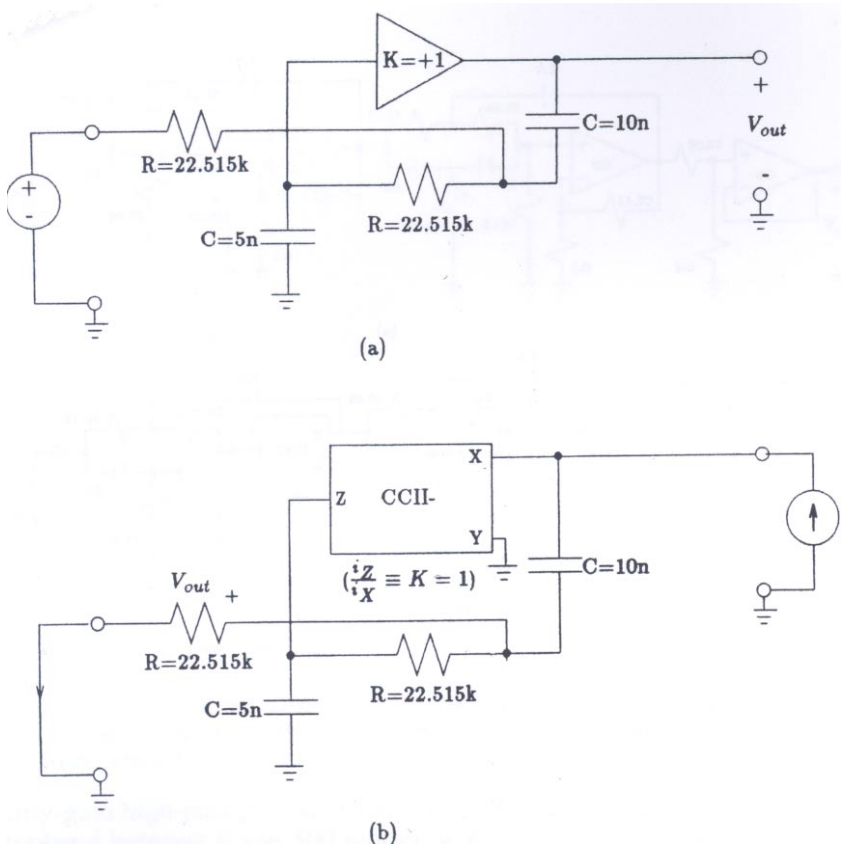


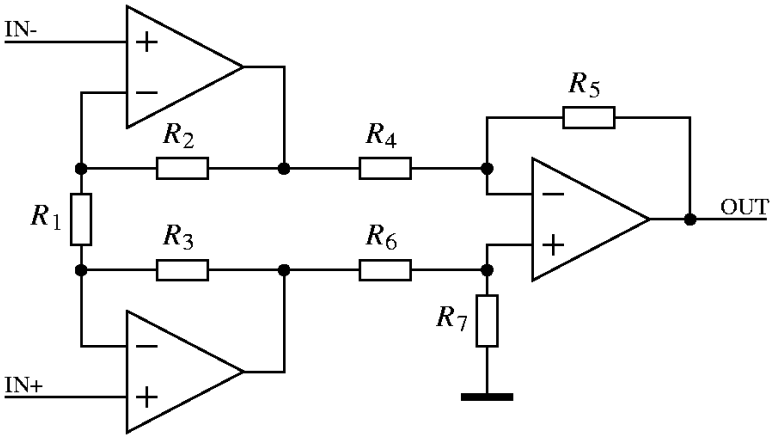

**Fig. 20** *Ideal and measured frequency response of current amplifier based SAB circuit*

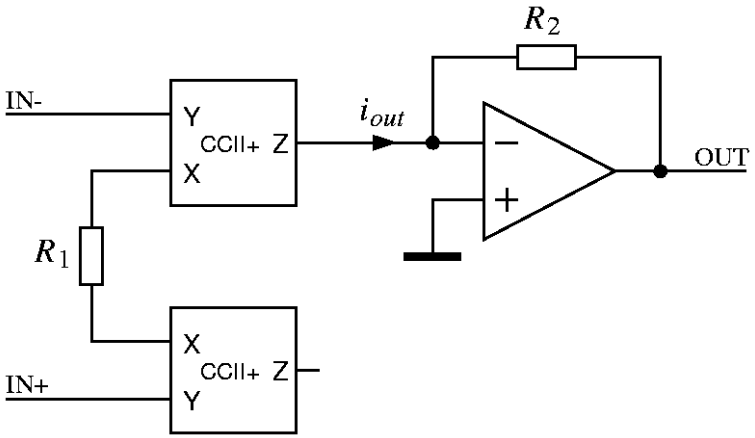
● = Measured
— = Ideal



# Instrumentation amplifier

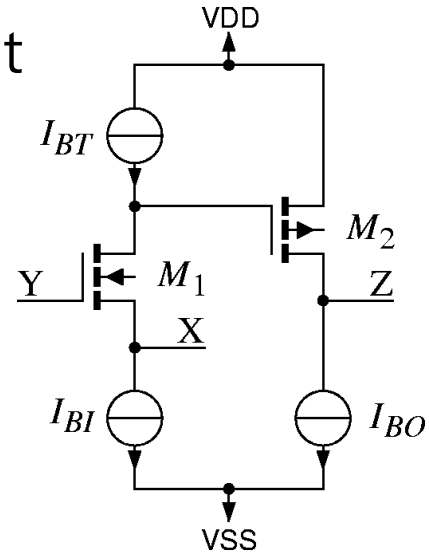
- Instrumantation amplifiers implemented with three op-amps requires several matched resistors to quarantee high CMRR
  - Because of the limited gain-bandwidth product of the high-gain amplifiers the bandwidth of the CMRR is limited
- A differential amplifier with high CMRR can be also realised with two current conveyor and two resistors without any matching components
  - The bandwidth of the current conveyor based amplifier is large with high voltage gains as current conveyors operate in open-loop without the gain-bandwidth product limitation

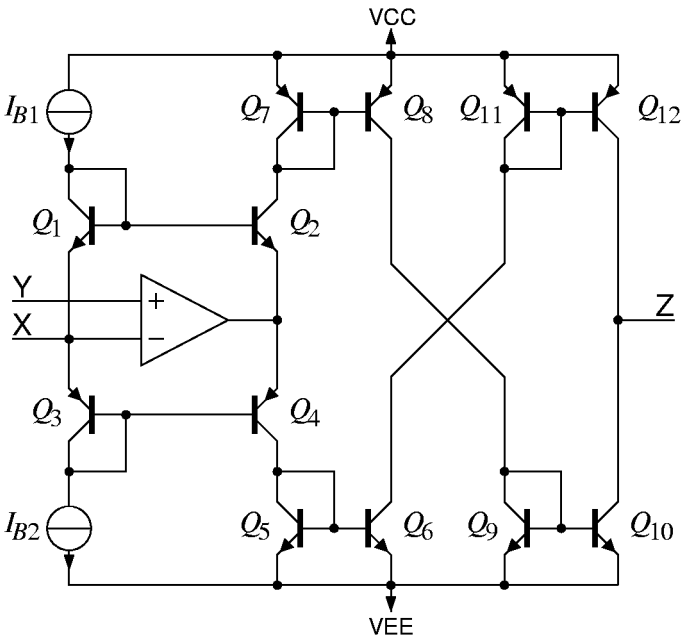


# High-gain current-conveyor CCII∞

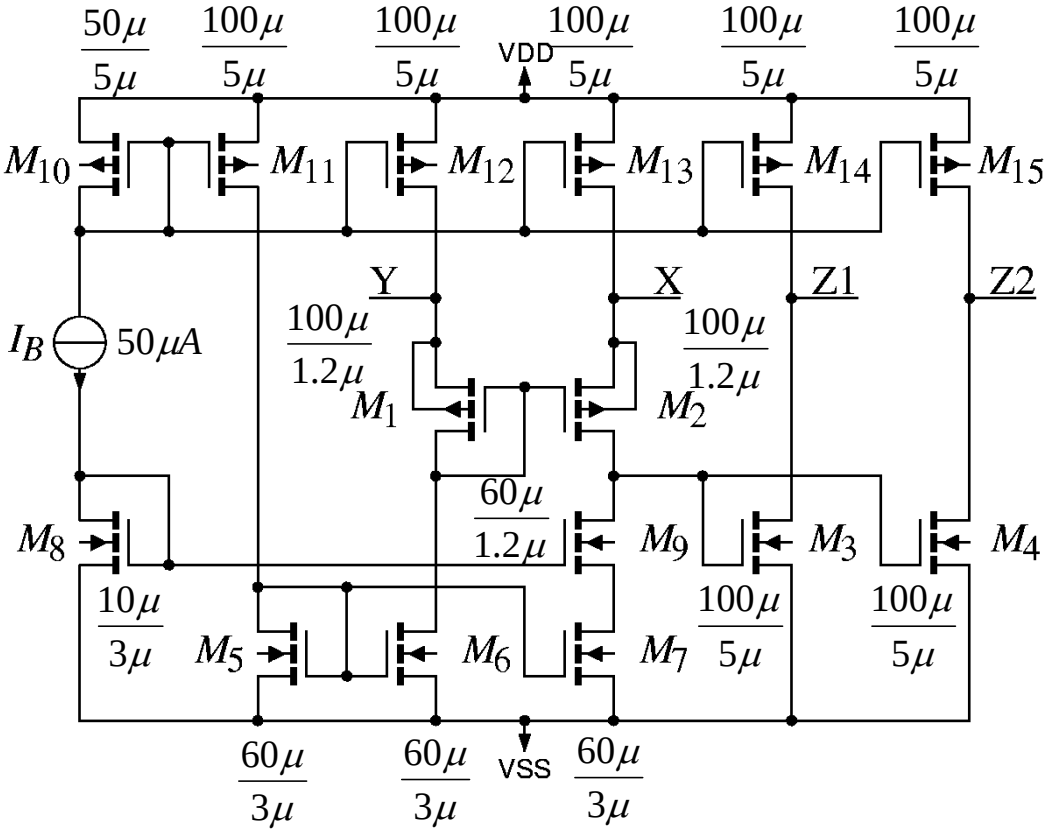
- Second-generation current-conveyor with very high forward current gain from X to Z
- Constructed with a CCII- and a transconductance output buffer
- Fully bipolar realisations are more complex than conventional bipolar voltage mode op-amp

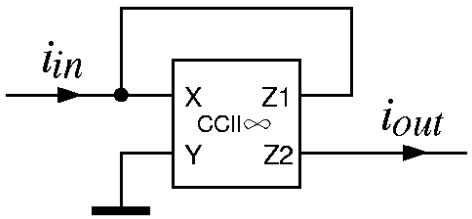


# CCII∞ in a 1.2µm n-well CMOS-process (1/3)

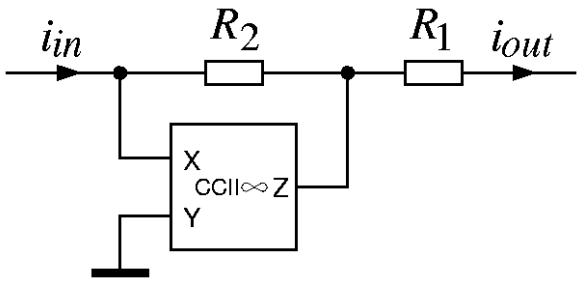
- Can be used as a drop-in replacement for op-amps in some applications
- PMOS input voltage follower maximises input voltage range but is not optimal for high-frequency operation
  - Larger parasitic capacitance due to the floating nwell
- Two identical outputs provide an unity current gain option
  - Closed-loop CCII∞ = CCII+



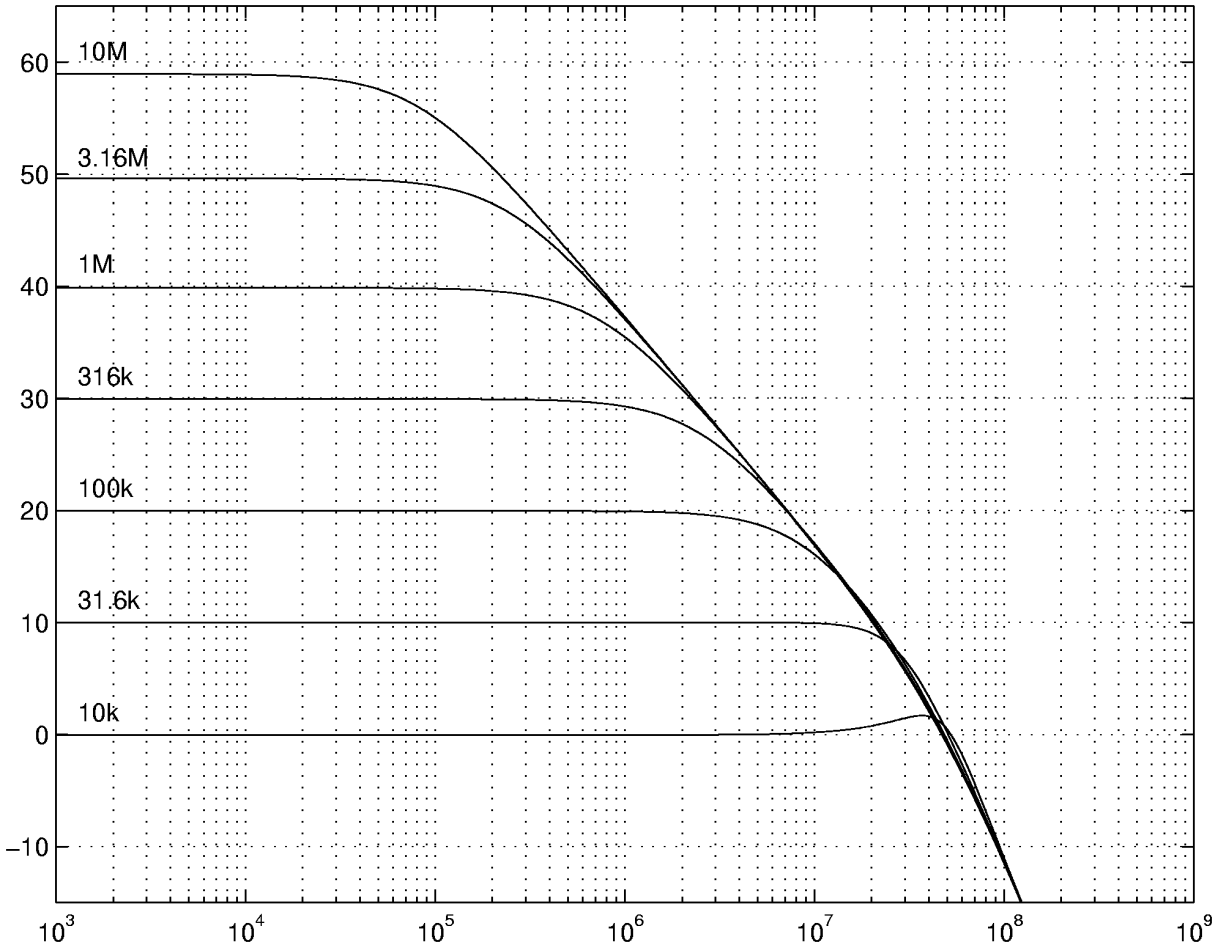



# CCII∞ in a 1.2µm n-well CMOS-process (2/3)

- **Closed-loop current amplifier**
- $Z_1$ and $Z_2$ connected together to form one output
- $R_2$ varied from 10kΩ to 10MΩ
- Load resistor $R_1$ is kept constant (10kΩ)

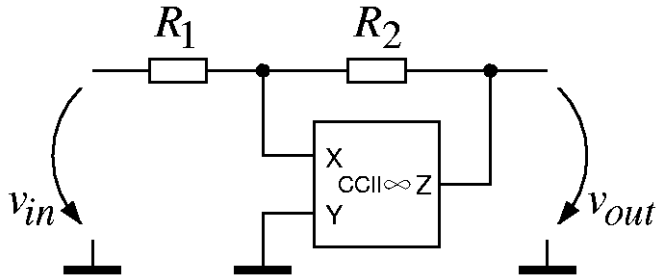



$$A_{icl}(0) \approx -\frac{R_2}{R_1}$$

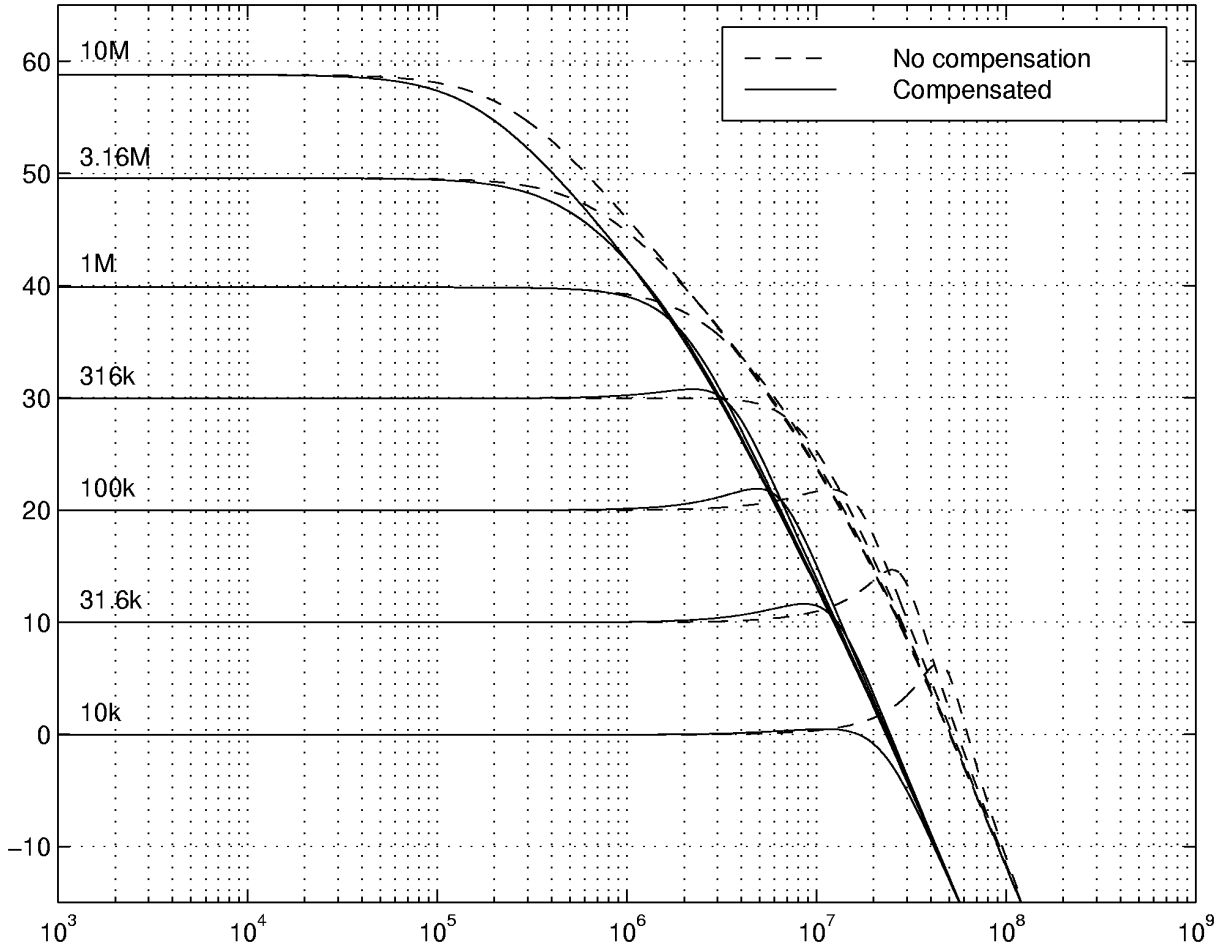


# CCII∞ in a 1.2µm n-well CMOS-process (3/3)

- **Closed-loop current amplifier**
- $Z_1$ and $Z_2$ connected together to form one output
- Input resistor $R_1$ is kept constant (10kΩ)
- A 5pF capacitor is connected to the gates of $M_3$ and $M_4$ to compensate the peaking

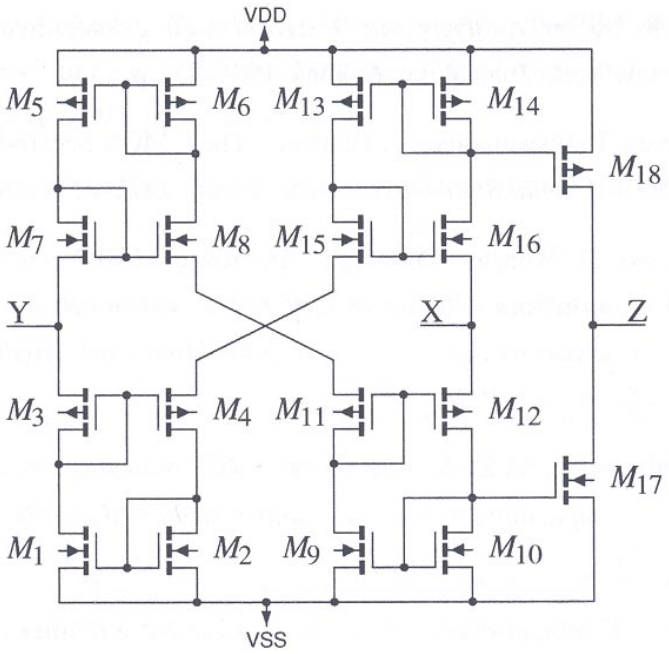



$$A_{vcl}(0) \approx -\frac{R_2}{R_1}$$

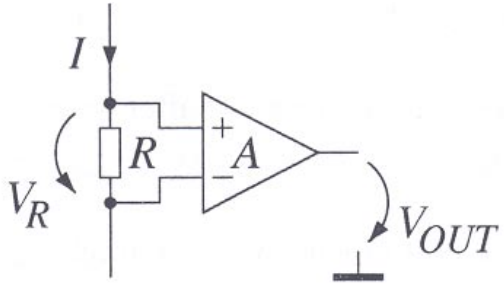


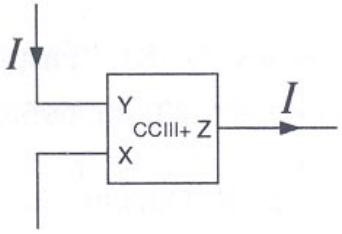
# Third generation current conveyor CCIII

- Published by Fabre in 1995
- Similar to CCI with the exception that the current in port X and Y flow in opposite directions
- Push pull topology built from four simple CCI
- Current measurement is the main application
  - The measurement with a shunt resistor and an operational amplifier can be problematic if the resistor should be low




$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}$$



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